We claim:

1. A method of analyzing a repair strategy for applying spare memory resources to a memory-under-test, comprising:

testing words of the memory-under-test for one or more defects, the testing being performed at an operating speed of the memory-under-test;

updating a record of column defects at substantially the operating speed of the memory-under-test, the record of column defects indicating the defects not repaired by spare rows; and

evaluating the record of column defects after the testing to determine whether the memory-under-test is repairable using the repair strategy.

2. The method of claim 1, wherein multiple defects are found in a word tested, and the record of column defects is updated to include the multiple defects.

3. The method of claim 1, further comprising sending row-address information and column-address information to external test equipment if the evaluating determines that the memory-under-test is repairable using the repair strategy.

4. The method of claim 1, wherein the record of column defects comprises a set of bits, each bit in the set corresponding to a respective column in the memory-under-test and having a value indicative of whether a defect was found in the respective column.

5. The method of claim 1, wherein the record of column defects comprises a column repair vector comprising a series of bits stored in memory elements, each bit in the series corresponding to a respective column in the memory-under-test.

6. The method of claim 1, wherein the record of column defects is updated by logically ORing a failure map from a word-under-test with at least a portion of the current record of column defects.

7. The method of claim 1, wherein the updating is performed if a current spare resource is a spare column and if the one or more defects from a current word being tested are not found in a current record of column defects or are not covered by a previously allocated spare row resource.

8. The method of claim 1, wherein the memory-under-test is a multiplexed memory, and wherein the record of column defects comprises one or more word-oriented records each associated with a different word position in the multiplexed memory.

9. The method of claim 8, wherein each word-oriented record comprises a set of bits, a first portion of the set corresponding to respective columns in the memory-under-test and a second portion of the set corresponding to word-position information.

10. The method of claim 9, wherein the number of bits comprising the one or more word-oriented records is less than the number of bits in a row of the memory-under-test.

11. A method of testing an embedded memory of an integrated circuit, wherein the method of claim 1 is performed simultaneously for multiple different repair strategies.

12. A method of testing an embedded memory of an integrated circuit, wherein the method of claim 1 is performed sequentially for multiple different repair strategies.

13. An integrated circuit comprising a built-in self-repair analyzer configured to perform the method of claim 1.

14. A computer-readable medium storing computer-executable instructions for causing a computer system to at least partially design a built-in self-repair analyzer configured to perform the method of claim 1.

15. A computer-readable medium storing a design database that includes design information for a built-in self-repair analyzer configured to perform the method of claim 1.

16. A method for performing a self-repair analysis of a memory, the memory comprising a plurality of memory cells arranged into rows and columns, the method comprising:

receiving a failure map associated with a test of a word in the memory, the word of the memory comprising at least two memory cells from a respective row of the memory, each memory cell of the word corresponding to a different column in the respective row;

determining which columns in the word have a defect based on the failure map; and

evaluating a current spare resource if one or more defects are found in the word and are not already covered by either a record of column defects or a committed spare row resource, the act of evaluating comprising,

logically updating the record of column defects with the failure map to include the one or more defects if the current spare resource is a spare column, and

advancing the current spare resource to a next spare resource according to a selected repair strategy.

17. The method of claim 16, wherein the act of evaluating further comprises storing corresponding row information if the current spare resource is a spare row.

18. The method of claim 16, wherein the record of column defects comprises a set of bits, each bit of the set corresponding to a respective column of the memory and having a value indicative of whether a defect is found in the respective column during a memory test of multiple words in the memory.

19. The method of claim 16, wherein the record of column defects is a column repair vector comprising a set of memory elements, each memory element in the set corresponding to a respective column in the memory.

20. The method of claim 16, wherein the memory has a multiplexed architecture and the record of column defects comprises multiple word-oriented column repair vectors, wherein each word-oriented column repair vector comprises a set of memory elements, a first portion of the set corresponding to respective columns in the memory-under-test and a second portion of the set corresponding to word-position information.

21. The method of claim 16, wherein the record of column defects is updated by logically ORing the failure map with at least a portion of the record of column defects.

22. The method of claim 16, further comprising, determining whether the selected repair strategy is successful by evaluating the record of column defects as the record of column defects is updated.

23. The method of claim 16 performed simultaneously using multiple different repair strategies.

24. The method of claim 23, wherein the multiple repair strategies are analyzed using $(C(m+n, m) - 1)$ or fewer built-in self-repair analyzers.

25. The method of claim 16 performed sequentially using multiple different repair strategies.

26. An integrated circuit comprising a built-in self-repair analyzer configured to perform the method of claim 16.

27. A computer-readable medium storing computer-executable instructions for causing a computer system to at least partially design a built-in self-repair analyzer configured to perform the method of claim 16.

28. A computer-readable medium storing a design database that includes design information for a built-in self-repair analyzer configured to perform the method of claim 16.

29. A method for repairing a memory using multiple repair strategies, comprising:

in a first test of the memory, analyzing defects in the memory using a first repair strategy, the first repair strategy comprising a predetermined order of spare resources that are applied sequentially to the defects of the memory;

determining if the memory is repairable using the first repair strategy;

if the first repair strategy fails to repair the memory, identifying a failing portion of the first repair strategy corresponding to a sequence of the spare resources applied to the defects of the memory before the first repair strategy failed; and

eliminating from subsequent tests of the memory one or more other repair strategies that begin with the failing portion of the first repair strategy.

30. The method of claim 29, wherein the first test of the memory comprises:

testing words of the memory at an operating speed of the memory; and

updating a record of column defects at substantially the operating speed of the memory-under-test, the record of column defects indicating the defects not assigned to be repaired by spare rows.

31. The method of claim 29, wherein the determining is performed as the spare resources of the first repair strategy are being applied to the defects of the memory.

32. The method of claim 29, wherein the determining is performed by evaluating a record of column defects.

33. The method of claim 32, wherein the record of column defects is a column repair vector comprising a set of bits, each bit in the set corresponding to a respective column in the memory.

34. The method of claim 29, wherein the memory has a multiplexed architecture and the record of column defects comprises multiple word-oriented column repair vectors, wherein each word-oriented column repair vector comprises a set of bits, a first portion of the set corresponding to respective columns in the memory-under-test and a second portion of the set corresponding to word-position information.

35. An integrated circuit comprising a built-in self-repair analyzer configured to perform the method of claim 29.

36. A computer-readable medium storing computer-executable instructions for causing a computer system to at least partially design a built-in self-repair analyzer configured to perform the method of claim 29.

37. A computer-readable medium storing a design database that includes design information for a built-in self-repair analyzer configured to perform the method of claim 29.

38. An integrated circuit, comprising:

a memory array comprising a plurality of memory cells, the memory cells being arranged into rows and columns, at least some of the rows in the memory array comprising one or more memory words formed from m memory cells, where m is an integer greater than or equal to two;

at least two spare memory resources, the at least two spare memory resources comprising one or more spare memory columns assignable to repair faulty columns in the memory array and one or more spare memory rows assignable to repair faulty rows in the memory array;

a built-in self-test (BIST) circuit configured to generate and apply test patterns to the memory words of the memory array and to generate failure maps and address information for the memory words tested; and

a built-in self-repair analyzer (BISRA) coupled to the BIST circuit and configured to receive the failure map and the address information for the memory words tested and to evaluate one or more repair strategies for applying the spare resources to the memory array,

the BISRA comprising a set of at least *n* memory elements that form a record of column defects, at least some of the *n* memory elements corresponding to respective columns of the words tested and having values indicative of whether a defect is found in the corresponding column.

39. The integrated circuit of claim 38, wherein *m* is equal to *n*.

40. The integrated circuit of claim 38, wherein the set of memory elements is logically updated with a respective failure map when a respective word tested contains a defect to be repaired with a spare column.

41. The circuit of claim 38, wherein the one or more repair strategies comprise a first repair strategy and a second repair strategy, and wherein the BISRA is configured to restart the BIST circuit if the first repair strategy fails and to evaluate the second repair strategy.

42. The circuit of claim 38, wherein the one or more repair strategies are a plurality of repair strategies, and the BISRA is configured to evaluate the plurality of repair strategies sequentially.

43. The circuit of claim 42, wherein the plurality of repair strategies are generated by hardware in the BISRA.

44. The circuit of claim 43, wherein the hardware in the BISRA generating the plurality of repair strategies comprises a linear feedback shift register (LFSR).

45. The circuit of claim 38, wherein the BISRA is a first BISRA of multiple BISRAs and the one or more repair strategies are a plurality of repair strategies, the multiple BISRAs being configured to evaluate the plurality of repair strategies simultaneously.

46. The circuit of claim 45, further comprising a determination circuit configured to select an optimal repair strategy from successful repair strategies evaluated by the first BISRA and the additional BISRAs.

47. The integrated circuit of claim 38, wherein the one or more repair strategies are loaded from automatic test equipment (ATE).

48. The circuit of claim 38, wherein the memory array has a linear architecture.

49. The circuit of claim 38, wherein the memory array has a multiplexed architecture and the set of memory elements comprises multiple word-oriented column repair vectors, each word-oriented column repair vector comprising a first subset of memory elements associated with word-address information and a second subset of memory elements associated with the respective columns of the words tested and having values indicative of whether defects are found in the corresponding columns.

50. The circuit of claim 49, wherein n is less than m.

51. The circuit of claim 49, wherein n is less than $m/2$.

52. A computer-readable medium storing computer-executable instructions for causing a computer system to at least partially design the integrated circuit of claim 38.

53. A computer-readable medium storing a design database that includes design information for the integrated circuit of claim 38.

54. An integrated circuit, comprising:

a word-oriented memory;

means for testing words of the memory at an operating speed of the memory and evaluating one or more spare resources according to a repair strategy, each of the one or more spare resources comprising either a spare row or a spare column; and

means for updating a record of column defects when a current spare resource being evaluated is a spare column and when one or more defects detected are not recorded in the record of column defects, the record of column defects being updated at substantially the operating speed of the memory.

55. The integrated circuit of claim 54, further comprising means for evaluating the record of column defects after the testing is performed to determine whether the memory is repairable using the repair strategy.

56. A computer-readable medium storing computer-executable instructions for causing a computer system to at least partially design the integrated circuit of claim 54.

57. A computer-readable medium storing a design database that includes design information for the integrated circuit of claim 54.